WHAT IS CLAIMED IS:

1. A memory control device for controlling a memory unit, wherein the memory unit includes at least a memory bank and the memory bank includes graphic memory, the control device comprising:

a command decoding device for receiving a memory access command and a bank address range signal, wherein the memory access command includes an access address and a command code, the command decoding device determines the memory bank range of the access address according to a bank address range signal and outputs a memory bank number signal, and the command decoding device outputs a partial write signal according to the command code;

a compare logic device coupled to the command decoding device, wherein the compare logic device determines if the access address resides within a memory bank range with error-check-correction function according to the memory bank number signal and an error-check-correction bank number signal and finally outputs an error-check-correction bank signal;

a frame buffer decode device for receiving the memory access command and a frame buffer range signal and determining if the access address falls within the graphic memory range and finally outputs a frame buffer access signal;

a decision device coupled to the command decoding device, the compare logic device and the frame buffer decode device for outputting an error-check-correction calibration enable signal and a read-modify-write enable signal according to the partial write signal, the error-check-correction bank signal and the frame buffer access signal; and

a command routing device coupled to the decision device for executing a memory read-modify-write program according to the read-modify-write enable signal;

wherein when the access address points to a memory bank range having an error-check-correction function and also within the graphic memory range, data is read from the memory or written to the memory without executing an error-check–correction function.

2. The memory control device of claim 1, wherein the device further includes a frame buffer range device for outputting the frame buffer range signal to the frame buffer decode device, and the frame buffer range signal relates to the address range of the graphic memory.

3. The memory control device of claim 1, wherein the decision device further includes:

an inverter for receiving the frame buffer access signal;

a first AND gate, wherein a first input terminal of the first AND gate receives the error-check-correction bank signal and a second input terminal of the first AND gate receives the partial write signal;

a second AND gate, wherein a first input terminal of the second AND gate is coupled to the output terminal of the inverter, a second input terminal of the second AND gate receives the error-check-correction bank signal and an output terminal of the second AND gate outputs the read-modify-write enable signal; and

a third AND gate, wherein a first input terminal of the third AND gate is coupled to the output terminal of the inverter, a second input terminal of the third AND gate is coupled to the output terminal of the second AND gate, and an output terminal of the third AND gate outputs the error-check-correction calibration enable signal.

4. The memory control device of claim 1, wherein the memory access command is provided by a graphic engine.

5. The memory control device of claim 1, wherein the device further includes a calibration unit coupled to the memory for determining whether to perform an error-check-correction calibration of the data read from the memory according to the error-check-correction calibration enable signal, and a data register for receiving data from the calibration unit and transmitting the data to the graphic engine.

6. A memory control method for controlling the transfer of memory data, comprising:

receiving and decoding a memory access command, wherein the memory access command includes an access address and a command code;

if the access address points to a memory bank range having an error-check-correction function but outside a graphic memory range:

reading data from memory and modifying the data before writing back into the memory if the command code is a partial write command; and

executing an error checking and correction program while reading from the memory if the command cod is a read command;

writing the data to memory if the command code is a normal write command; and

if the access address is within the graphic memory range, conducting a read/write operation without any error checking or correction.

7. The memory control method of claim 6, wherein determining the actions on the memory further includes:

if the command code is a partial write command, data is read from the memory and modified before writing back;

if the command code is a non-partial write command, a normal memory write operation is conducted; and

if the command code is a read command, a data read from the memory read is error-checked and corrected.

8. A memory control method for controlling the transfer of memory data, comprising:

receiving and decoding a memory access command, wherein the memory access command includes an access address and a command code; and

disabling an error-check-correction function if the access address points to a memory bank range having an error-check-correction function and inside a frame buffer range.